REMARKS

Claims 1-6, 16-19, and 31-40 are pending. Of these, Applicants thank the Examiner for the indication that claims 37-40 are allowed.

For the following reasons, reconsideration of the rejection is respectfully requested.

REJECTION UNDER 35 U.S.C. §103:

On page 2 of the Office Action, claims 1-6, 16-19, and 31-36 are rejected under 35 U.S.C. §103(a) as being unpatentable over Miyazawa et al. (EP 0465961), in view of Egawa (JP 7-273340), and further in view of Chau et al. (U.S. Patent 6,653,700). The rejection is respectfully traversed.

It is respectfully submitted that the combination of Miyazawa, Egawa, and Chau, fails to render obvious a thin film transistor, comprising an active layer formed on an insulating substrate and having channel, source, and drain regions formed therein, wherein a voltage is applied to the channel region to discharge hot carriers generated in the channel region and the channel region is an intrinsic region, as recited in claim 1.

Also, the combination of Miyazawa, Egawa, and Chau, fails to render obvious a flat panel display, comprising a gate line, a data line and a power supply line, and a plurality of pixels connected to the lines, wherein each of the pixels comprises one or more thin film transistors comprising channel, source, and drain regions in an active layer, and a voltage is applied to the channel region of the thin film transistor to discharge hot carriers, and the channel region is an intrinsic region, as recited in claim 16.

Also, the combination of Miyazawa, Egawa, and Chau, fails to render obvious an active layer of a thin film transistor, the active layer comprising, a source region, a drain region, a channel region, and a bias supply region to supply a voltage to the channel region to discharge hot carriers wherein the channel region is an intrinsic region, as recited in claim 31.

Also, the combination of Miyazawa, Egawa, and Chau, fails to render obvious a thin film transistor, wherein a voltage is applied to a channel region by a member other than a gate electrode, and wherein the voltage discharges hot carriers generated in the channel region, and the channel region is an intrinsic region, as recited in claim 33.

Specifically, it is respectfully submitted that there is no suggestion or motivation to modify the structures of Miyazawa and Egawa with the intrinsic channel of Chau because the proposed modification requires changes that would render both Miyazawa and Egawa unsatisfactory for their intended purposes (see, Manual of Patent Examination Procedure (MPEP §2143.01(V)) at page 2100-129, rev. 5, Aug. 2006).

Specifically, Chau discloses a transistor 200 having a very thin intrinsic or undoped epitaxial silicon body or channel 208 that is formed on an insulating substrate (see, col. 2, lines 35-37, and FIG. 2 of Chau). As shown, the channel 208 is formed between sources/drains 230, and below a gate dielectric layer 210. The gate dielectric layer 210, in turn, is formed below a gate electrode 212 that includes a mid-gap work function film 214 and a heavily doped polysilicon film 216, among others (see, col. 2, lines 44-56, and FIG. 2 of Chau).

A pair of sidewall spaces 218 is formed to isolate the gate electrode 212, that includes the mid-gap work function film 214, from the doped silicon or silicon alloy film 220 of the sources/drains 230 (see, col. 3, lines 4-9, lines 21-23, and FIG. 2 of Chau). Chau further discloses that the mid-gap work function film 214 is formed of metal, metal nitride, or metal silicide (see col. 2, lines 60-66 of Chau). As a preferred embodiment, Chau discloses that the mid-gap work function film 214 is titanium nitride. Titanium nitride is known as a barrier metal and a good electrical conductor.

Chau discloses that the undoped channel or body 208 is used to enable a transistor 200 to have a low threshold voltage, but Chau insists that the use of the undoped channel or body 208 also <u>requires</u> use of the mid-gap work function film 214 as the lower layer of the gate electrode film 212 (see, col. 3, line 67-col. 4, line 7 of Chau). That is, if the undoped channel or body 208 of Chau is to be used, Chau requires that the mid-gap work function film must also be used to raise the threshold voltage of the device (see, col. 4, line 3-7 of Chau).

Accordingly, one of ordinary skill in the art, when contemplating combining the undoped channel or body 208 of Chau with Miyazawa and/or Egawa, is taught to also use the mid-gap work function film 212 of Chau. However, one of ordinary skill in the art would quickly realize that the required mid-gap work function film 214, when worked into Miyazawa and/or Egawa, would cause a short between the drain/source regions thereof because the mid-gap work function film 214 must be located as the lower layer of the gate electrode film. In the case of Miyazawa, such would locate the mid-gap work function film 214 below the gate insulating film 7 (see, for example, FIG. 3 of Miyazawa), and in the case of Egawa, such would locate the mid-

gap work function film 214 below the gate dielectric film 8 (see, for example, FIG. 2 of Egawa). However, it is readily observable that such placement of the mid-gap work function film 214 will cause a short between the source 5 and the drain 6 of Miyazawa (see, FIG. 3 of Miyazawa), and cause a short between the source/drain electrodes 6a of Egawa (see, FIG. 2 of Egawa).

Accordingly, the intended purpose of the Miyazawa MISFET, or the Egawa transistor, for example, would be destroyed if the undoped channel or body 208 of Chau is used because use of the undoped channel or body 208 of Chau requires use of the mid-gap work function film 214 that cause shorts. Thus, because the proposed modification requires changes that would render both Miyazawa and Egawa unsatisfactory for their intended purposes, there cannot be motivation to combine the references, and the proposed combination is improper.

Accordingly, claims 1, 16, 31, and 33 are not obvious over the applied references and their combination because of the lack of motivation to combine the references. Also, claims 2-6 and 34, which depend from claim 1, claims 17-19 and 35, which depend from claim 16, claim 32 and 36, which depend from claim 31, are likewise not obvious over the applied references and their combination for at least the reasons discussed above, and for the additional features they recite. Withdrawal of the rejection is respectfully requested.

ALLOWABLE SUBJECT MATTER:

Claims 37-40 are allowed.

CONCLUSION:

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

STEIN, MCEWEN & BUI, LLP

Date: $\frac{3/16/2007}{}$

Dy. Soth S

Registration No. 54,577

1400 Eye St., N.W.

Suite 300

Washington, D.C. 20005 Telephone: (202) 216-9505 Facsimile: (202) 216-9510